PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		§	
	JOSHUA M. CONNER, ET AL.	§	Group Art No. **2183**
		§	
Serial No.:	**09/870,458**	§	
		§	
Filed:	**June 1, 2001**	§	Examiner: **Tonia L. Meonske**
		§	
For:	**MULTI-PRECISION BARREL SHIFTING**	§	Attorney Docket No.: **068354.1439**

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION MAILED FEBRUARY 15, 2006

Dear Sir:

In response to the Final Office Action mailed February 15, 2006, Applicants respectfully request reconsideration of the rejections set forth in the Office Action. The three-month shortened statutory time for response expires on May 15, 2006. Therefore, this Response is timely filed.

The **Claim Amendments** begin on page 2 of this Response.

The **Remarks** begin on page 6 of this Response.

LISTING OF THE CLAIMS

Claims 1-18 **(canceled)**

19. **(currently amended)** A method, implemented in a computer system, of shifting a multi-word value comprising:

performing a first shift operation on a first portion of the multi-word value to produce one or more overflow bits;

performing a second shift operation on a second portion of the multi-word value, where the second shift operation comprises:

producing a shift result; and

concatenating the shift result and the overflow bits~~.~~; and

where the second shift operation is a multi-precision shift instruction and where the first shift instruction and second shift instruction are performed sequentially.

20.(**previously presented)** The method of claim 19, where the second shift operation is a multi-precision shift instruction, and where the second shift operation produces a result, the method further comprising:

fetching and decoding the multi-precision shift instruction; and

outputting the result.

21. **(previously presented)** The method of claim 20, where the multi-precision shift instruction is a shift left instruction.

22. **(previously presented)** The method of claim 20, where the multi-precision shift instruction is a shift right instruction.

23. **(previously presented)** The method of claim 20, where the multi-precision shift instruction

specifies a shift increment.

24. **(previously presented)** The method of claim 23, where the shift increment is greater than or equal to the number of bits in a word.

25. **(previously presented)** The method according to claim 23, where the shift increment is less than the number of bits in a word.

26. **(previously presented)** The method of claim 19, further comprising:

storing one or more bits shifted out of the second portion of the multi-word value during the second shift instruction in a carry register.

27. **(previously presented)** The method of claim 19, where concatenating the shift result and the overflow bits comprises:

performing a logical OR operation on at least one bit in the shift result and at least one overflow bit.

28. **(previously presented)** The method of claim 19, further comprising:

storing one or more of the overflow bits in a carry register.

29. **(previously presented)** A processor for processing multi-precision shift instructions, comprising:

a program memory for storing instructions including at least one multi-precision shift instruction;

a program counter for identifying current instructions for processing; and

a barrel shifter for executing shift instructions, including the at least one multi-precision shift instruction, the barrel shifter including:

one or more carry registers for storing values shifted out of sections of the barrel shifter; and

OR logic for concatenating values stored in one or more carry registers with values in the barrel shifter; and

where the barrel shifter is operable to shift a multi-word value, and where when shifting a multi-word value the barrel shifter:

executes at least one shift instruction to:

load a first operand into a section within the barrel shifter, where the first operand is a first portion of the multi-word value; and

generate one or more overflow bits; and

executes at least one multi-precision shift instruction fetched from the program memory to:

load a second operand into a section within the barrel shifter, where the second operand is a second portion of the multi-word value;

shift the second operand;

concatenate the second operand with one or more of the overflow

bits; and

output the shifted value.

30. **(previously presented)** The processor of claim 29, where the multi-precision shift instruction is a shift left instruction.

31. **(previously presented)** The processor of claim 29, where the multi-precision shift instruction is a shift right instruction.

32. **(previously presented)** The processor of claim 29, where the multi-precision shift instruction is an arithmetic shift instruction.

33. **(previously presented)** The processor of claim 29, where the multi-precision shift instruction is a logical shift instruction.

34. **(previously presented)** The processor of claim 29, where the multi-precision shift instruction specifies a shift increment.

REMARKS

Claims 19-34 were pending in the application before this Office Action. Claims 19 has been amended in this Response. Claims 19-34 are pending.

All amendments are made in a good faith effort to advance the prosecution on the merits. Applicants reserve the right to subsequently take up prosecution on the claims as originally filed in this or appropriate continuation, continuation-in-part and /or divisional applications.

Rejections under § 102

Claims 19-26 and 28 were rejected under 35 U.S.C. § 102(b) as anticipated by Intel's Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual. Applicants have again amended claim 19 to show that the first and second shift operations are separate sequential shift operations, unlike the double-shift instructions of Intel. Applicants therefore request reconsideration of claims 19-28.

Rejections under § 103

Claims 27 and 29-34 were rejected under 35 U.S.C. § 103(a) as unpatentable over Intel and U.S. Patent No. 6,314,200 to Silverbrook.

First, claim 27 depends from claim 18, which Applicants have shown to be patentable above. Applicants therefore respectfully request the withdrawal of the rejection of claim 27.

> The Office Action states that:
>
> 25. Referring to claim 29, Intel has taught a processor for processing multi-precision shift instructions, comprising:
>
> a. a program memory for storing instructions including at least one multi-precision shift instruction (Page 3-2, lines 1-3);
>
> b. a program counter for identifying current instructions for processing (page 3-15, section 3.3.5, Instruction Pointer), and
>
> c. a barrel shifter for executing shift instructions (Page 4-16 and 4-17), including the at least one multi-precision shift

> instruction (Pages 4-16 and 4-17, SHLD and SHRD), the barrel shifter including:
>
> i. one or more carry registers for storing values shifted out of sections of the barrel shifter (Page 4-16 and 4-17, CF); and logic for concatenating values stored in one or more carry registers with values in the barrel shifter (pages 25-289 to 25-292); and
>
> d. where the barrel shifter is operable to shift a multi-word value (Pages 4-16 and 4-17, SHLD and SHRD shift doubleword operands), and where when shifting a multi-word value the barrel shifter:
>
> 1. executes at least one shift instruction to:
>
> (1) load a first operand into a section within the barrel shifter, where the first operand is a first portion of the multi-word value (Pages 4-16 and 4-17, The source operand is loaded into the source register.); and
>
> (2) generate one or more overflow bits (Pages 4-16 and 4-17, Bits are shifted out of the source register.); and
>
> e. executes at least one multi-precision shift instruction fetched from the program memory (Pages 4-16 and 4-17, The SHRD and SHLD instruction are executed.) to:
>
> i. load a second operand into a section within the barrel shifter, where the second operand is a second portion of the multi-word value (Pages 4-16 and 4-17, The destination operand is loaded into the destination register.);
>
> ii. shift the operand; concatenate the operand with one or more of the overflow bits (Pages 4-16 and 4-17, A lower portion of bits of the destination are concatenated with the bits shifted out of the source register.); and
>
> iii. output the shifted value (Pages 4-16 and 4-17, The result is stored back into, or output to the destination operand.).

Office Action, pages 3-4.

Applicants respectfully disagree and contend that the combination of Intel and Silverbrook, assuming such a combination were possible, fails to teach each of the elements of claim 29. Claim 29 requires "a barrel shifter for executing shift instructions." Intel, however, does not disclose any structure for it's double word shifter, and the Office Action does not show that a barrel shifter structure is inherent. Each of claims 30-34 depend from claim 29, and are

similarly not obvious over the combination of Intel and Silverbrook. Applicants therefore respectfully request reconsideration of claims 30-34.

SUMMARY

Should the Examiner have any questions, comments or suggestions in furtherance of the prosecution of this application, the Examiner is invited to contact the attorney of record by telephone or facsimile.

Applicants believe that no fees are due at this time. If the Commissioner deems any additional fee is due, the Commissioner is hereby requested to accept this as a Petition therefore, and is authorized to charge any fees due, including any fees for an extension of time, to Baker Botts L.L.P. (formerly, Baker & Botts, L.L.P.) Deposit Account number 02-0383, Order number 068354.1439.

Respectfully submitted,

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